UNIVERSITY OF SA

College of Eng

Department of Electri

E.E. 432.3/E.

VLSI Circuit Design

Instructor: R.J. Bolton

MID-TERM EXAMINATION

February 14, 2002

7:00 PM - 9:00 PM

STUDENT NAME: _____

STUDENT NUMBER: _____

Question 1	15 / 15
Question 2	15 / 15
Question 3	14 / 15
TOTAL	44 / 45

GENERAL INSTRUCTIONS FOR THE QUESTIONS

1) OPEN E.E. 432.3/E.E. 451.3 textbook (**Principles of CMOS VLSI Design - A Systems Perspective by N.H.E. Weste and K. Eshraghian OR one other text**), OPEN E.E. 432.3/E.E. 451.3 notes, and OPEN E.E. 451.3 assignments.

2) NO library manuals (or copies thereof) ALLOWED! NO examination files ALLOWED!

3) Neatness counts. Please ensure your paper is readable.

4) Some questions contain special instructions. Please ensure that you read these carefully.

5) Not all questions are of the same difficulty and value. Consider this when allocating time for the solution.

6) *IF A QUESTION PROVES TO BE TOO HARD FOR YOU TO SOLVE, GO ON TO ANOTHER QUESTION! RETURN TO THE TROUBLESOME QUESTION WHEN TIME PERMITS.*

PLEASE NOTE

ALL parts of the examination paper MUST be handed in before leaving.

Please check that your examination paper contains 7 pages TOTAL.

SPECIFIC INSTRUCTIONS FOR THE EXAMINATION

1) All designs use standard CMOS3DLM design rules and layers. **V_{DD} = +5V and V_{SS} = 0V.**

2) Unless otherwise specified, normal substrate connections are assumed for all P-channel and N-channel transistors, i.e., V_{SS} for N-channel and V_{DD} for P-channel.

3) CMOS3DLM resistance and capacitance parameters are as follows:

Layer	Resistance	Capacitance
N-Diffusion	25.0 Ω/□	4.4E-4 pf/μm^2
P-Diffusion	80.0 Ω/□	1.5E-4 pf/μm^2
Polysilicon	18.0 Ω/□	6.0E-5 pf/μm^2
Metal 1	0.035 Ω/□	2.7E-5 pf/μm^2
Metal 2	0.030 Ω/□	1.4E-5 pf/μm^2
N-Transistor	4275 Ω/□	See below
P-Transistor	13600 Ω/□	See below
Gate-channel	See above	6.9E-4 pf/μm^2

4) Supplementary physical constants are as follows:

Constant	Symbol	Value	Units
Electron charge	q	1.602E-19	coulomb
Boltzmann's constant	k	1.38E-23	Joule/°K
Intrinsic carrier concentration of Si @ T=300°K (27°C)	n_i^2	2.1E+20	(carriers/cm^8)^2
Permittivity of free space	ε_0	8.854E-14	Farad/cm
Permittivity of Si	ε_{Si}	$11.7\varepsilon_0$	Farad/cm
Permittivity of SiO_2	ε_{ox}	$3.9\varepsilon_0$	Farad/cm

5) (H)SPICE process parameters are as follows:

Parameter	Name	N-channel	P-channel	Units
V_t	Zero-bias threshold voltage	0.7	-0.8	Volts
κ'	Process gain factor	40.0E-6	12.0E-6	A/V^2
γ	Bulk threshold body factor	1.1	0.6	V$^{1/2}$
$2\lvert\phi_F\rvert$	Surface potential	0.6	0.6	V
λ	Channel length modulation factor	1.0E-2	3.0E-2	1/V
t_{ox}	Oxide thickness	5.0E-6	5.0E-6	cm
N_A or N_D	Substrate doping density	1.7E+16	5.0E+15	1/cm^3
μ	Carrier surface mobility	775	250	cm^2/(V·sec)

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QUESTION #1

MARKS: 15 (3 + 3 + 3 + 3 + 3)

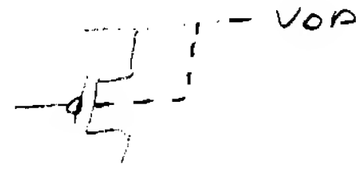
Indicate (in the space provided) whether the following are TRUE or FALSE. **Do any FIVE (5).** To obtain full marks for each question, include a ***SHORT*** sentence or two in support of your answer.

F 1) Enclosure design rules ensure that the gate area of a transistor is fabricated properly.

Overlap rules govern gate area fabrication

T 2) Substrate connections are used to make connections to the bulk terminal on MOS transistors.

The bulk terminal is connected to V_{DD} through the substrate, so it needs a substrate connection
- Shown w/ a dotted line in some schematics



T 3) Transmission gates are used to tri-state (or high-z) logic signals in sequential circuits.

No signal in gives a high output impedance. Not commonly used in industry because they're hard to test, however

T 4) Nortel and MITEL are two companies that do fabrication for the U of S.

- The CMC contracts them to do it.
  - Nortel - CMOS3D-M process
  - Mitel - MITEL process

→ acts as silicon broker

Mitel - recently discontinued the MITEL IS tech.

T 5) Self-aligned CMOS transistors are higher performance than metal gate CMOS transistors.

- Make sure there is no diffusion under the gate - polysilicon used as a mask
- polysilicon also has less resistance + capacitance per unit area ∴ it is faster

- better alignment - thinner tox
- metal gate → old technology → CD4000 series from RCA

F 6) The area of the wafer containing thin-oxide is also called a device well.

should be T

Device Wells are another name for diffusion - the gate is under the thin oxide

implies during fabrication → see app. C) p. C6

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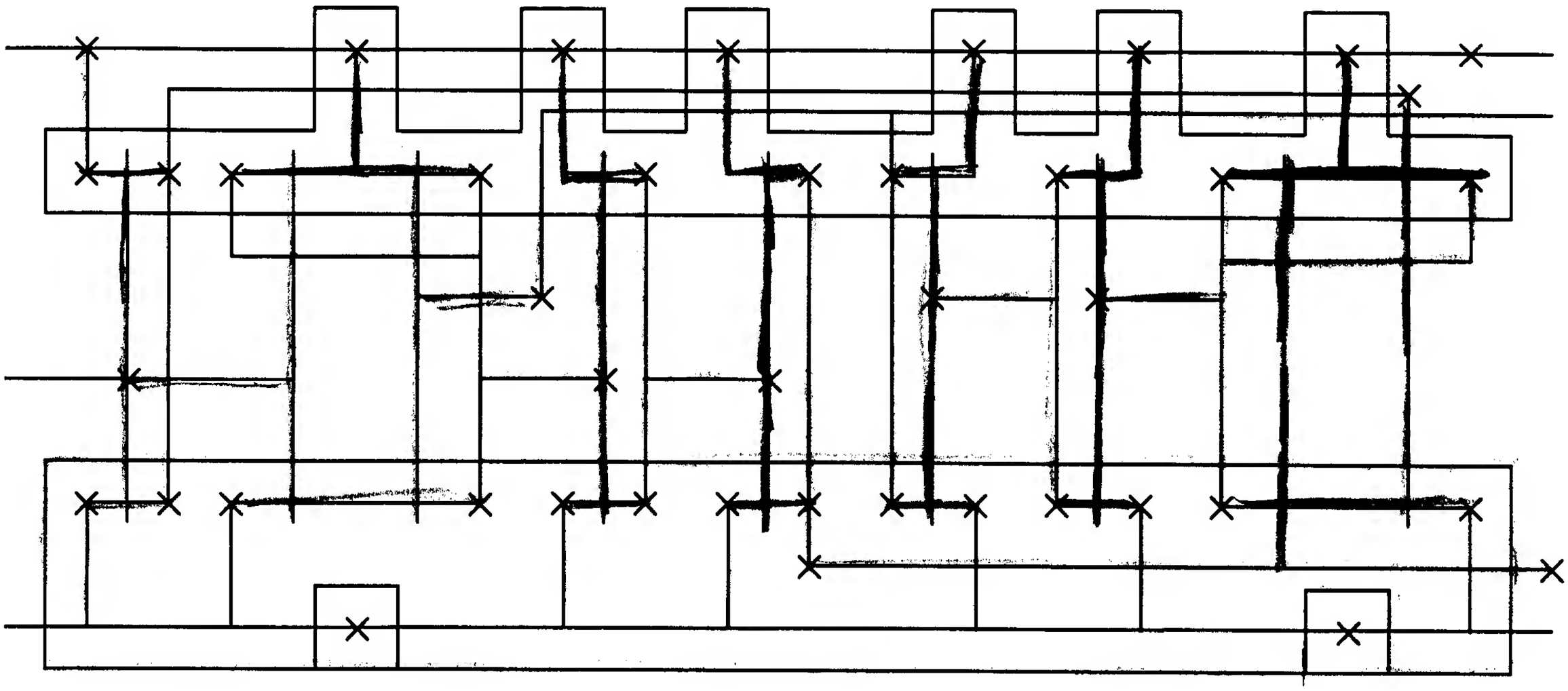
QUESTION #2

MARKS: 15 (10 + 5)

Consider the following plot of a CMOS3DLM STICKS layout shown below. Unfortunately it was plotted in black and white instead of color.



Use this STICKS layout as a spare or as a initial try for part a). Use the one on the following page as your final one (to assist you in doing part b) of this question).

Please note that the STICKS layout shown does not contain Metal 2 or Vias.

a) Using the following standard colors, color the STICKS layout (on the following page). Using the STICKS layout on the next page as your final one may facilitate doing part b) of this question.

CMOS3DLM Layer	Color
N+ diffusion	Green
P+ diffusion	Yellow/Orange
P+ mask	Dotted Orange
Polysilicon	Red
P-Well	Solid Brown
Metal 1	Blue
Metal 2	Black or Purple
Contact Cut	Black X
Via	Black O

No Metal 2
No Vias

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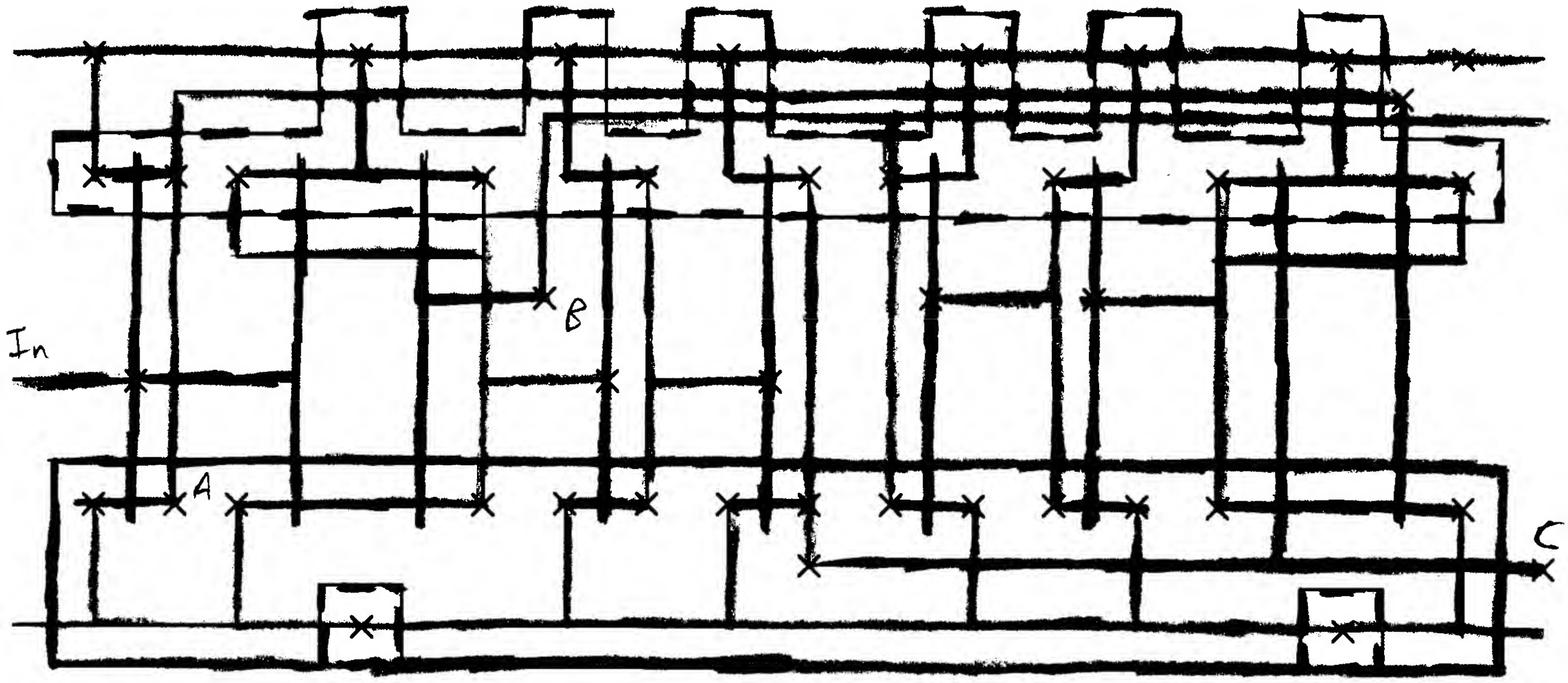
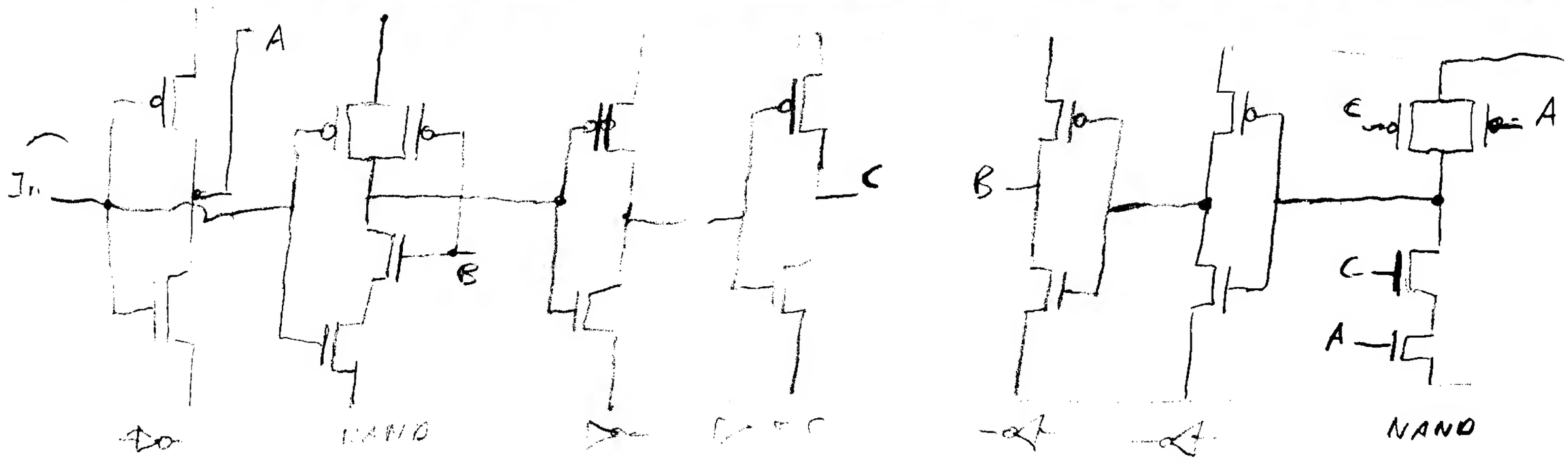
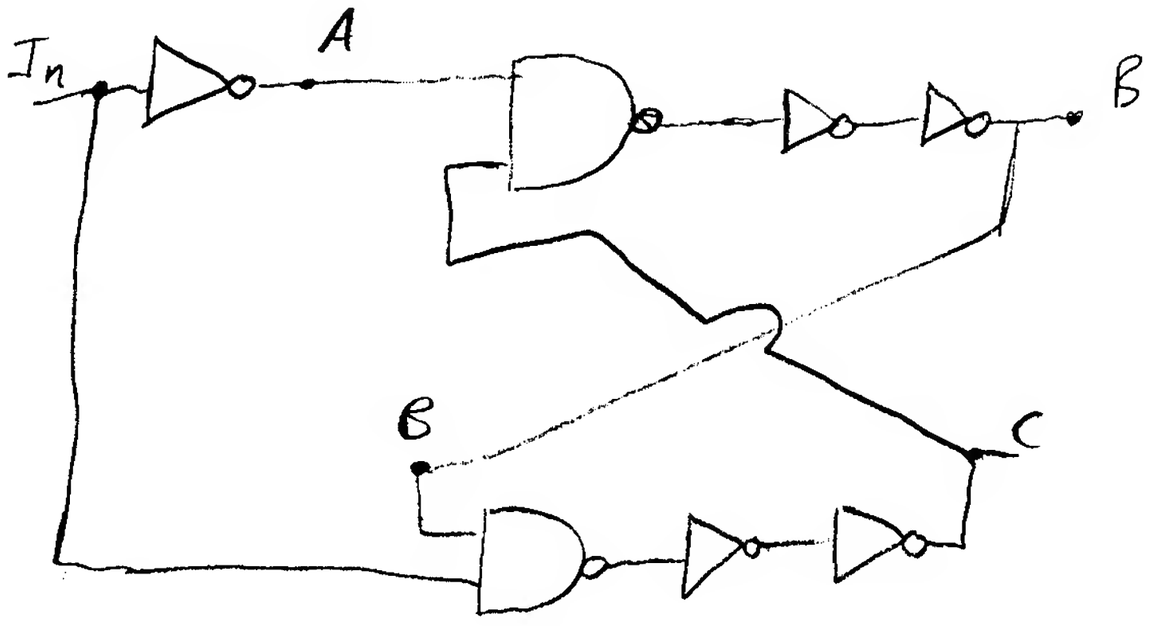
b) Draw a gate-level schematic of the STICKS circuit. Do NOT attempt to figure out what the circuit does (it will take too much time).

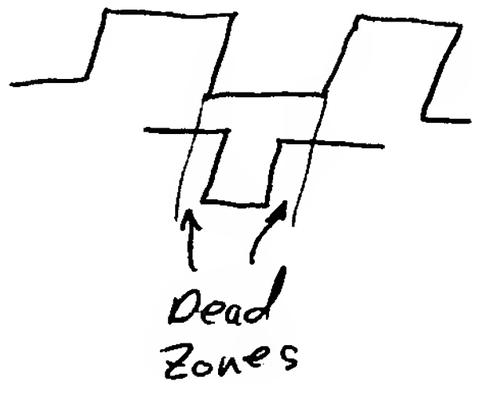






15

This is a correct two-phase clock generator. The two inverters in series set the node of the dead zone



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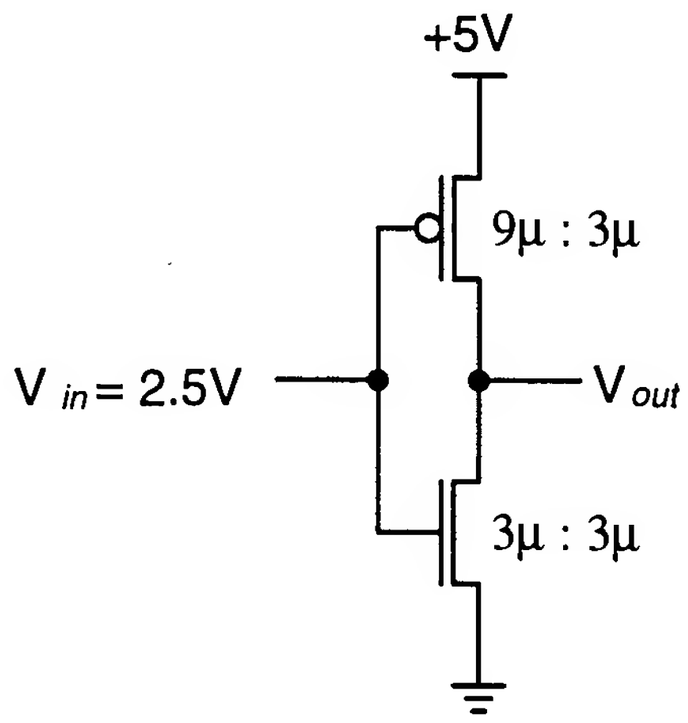
QUESTION #3

MARKS: 15 (15)

a) The following circuit is one of many standard designs for a CMOSDLM inverter. Calculate the output voltage, V_{out}, when the input voltage, V_{in}, is 2.5V. Important parameters are shown on Page 2. Show your calculation. Sizes shown are W:L.

You must state any assumption(s) that you make. **They must be reasonable, however!**



for a P transistor:

$V_{tp} = -0.8V$

for an N transistor:

$V_{tn} = 0.7V$

$\beta_N = 53.5\ \mu A/V^2 \left(\frac{W_N}{L_N}\right) = 53.5\ \mu A/V^2$

$\beta_P = 17.3\ \mu A/V^2 \left(\frac{W_P}{L_P}\right) = 51.9\ \mu A/V^2$

$\frac{\beta_N}{\beta_P} = 1.033$

$\frac{\beta_N}{\beta_P}$ is > 1. → This means the Vout vs. Vin curve is shifted to the left. Therefore the inverter is operating in the (D) region. (p device saturated, n device non-saturated)

For the (D) region:

$$V_{out} = (V_{in} - V_{tn}) - \sqrt{(V_{in} - V_{tn})^2 - \frac{\beta_p}{\beta_n}(V_{in} - V_{DD} - V_{tp})^2}$$

$$V_{out} = (2.5V - 0.7V) - \sqrt{(2.5V - 0.7V)^2 - \frac{1}{1.033}(2.5V - 5V + 0.7V)^2}$$

$V_{out} = 1.48\ V$

HIGH

1.14 V

-1

-1 ! should be 0.8

14

Question #3 Work Sheet

Student Name: _____ Student Number: _____